What is Claimed is:

1. In a data processing system transferring data cells between processing units using an asynchronous transfer mode Utopia protocol, an interface unit comprising:

apparatus for transferring data cells between the processing units, the transfer of data cells being controlled by an external clock signal; and

a clock detection unit for detecting the absence of the external clock signal, the clock detection unit generating a interface reset signal when the external clock signal is not detected.

2. The interface unit as recited in claim 1 wherein the clock detection unit includes a component for generating the interface reset signal when a external clock signal is not detected in a preselected time period.

3. The interface unit as recited in claim 2 wherein the component is a counter, the counter counting the internal clock signals, the preselected time period determined by the number of internal clock signals.

4. The interface unit as recited in claim 3 wherein the external clock signals are applied to a reset terminal of the counter.

5. The interface unit as recited in claim 4 wherein the interface unit is operating in a slave mode.

6. The interface unit as recited in claim 1, wherein the apparatus includes:

an input interface unit; and

an output interface unit; and wherein the buffer memory unit includes:

an input buffer memory unit, wherein the transfer between the input buffer memory unit and the direct memory access unit is determined by a receive event signal; and

an output buffer memory unit, wherein the transfer between the direct memory access unit and the output buffer memory unit is determined by a transmit event signal.

7 The interface unit as recited in claim 6 wherein the receive event signal is generated when the buffer memory unit has a complete data cell stored therein, the receive event signal being cleared when transfer between the buffer memory unit and the direct memory access unit is begun, and wherein the transmit event signal is generated when the buffer memory unit has space for a complete data cell, the transmit event signal being cleared when the transfer of the data cell to the buffer memory unit from the direct memory access unit is begun.

8. A method of insuring the accurate transmission of data through an interface unit acting in an asynchronous transfer mode, the interface unit having an external clock signal applied thereto, the method comprising:

determining when the external clock signal is present; and

when the external clock signal is not present, generating at least one control signal.

9. The method as recited in claim 8 wherein generating a control signal includes generating at least one of a reset signal and an interrupt signal.

10. The method as recited in claim 9 further comprising:

counting the number of signals of an internal clock;

resetting the count to zero by the external clock signals; and

when the count reaches a predetermined number, generating the at least one control signal.

11. The method as recited in claim 10 further comprising storing the predetermined number in a register.

12. An asynchronous transfer mode Utopia interface unit for providing a interface between an external data processing unit and a direct memory access unit, the interface unit comprising:

an input buffer memory unit, the input buffer memory unit providing data cells to the direct memory interface unit;

an interface input unit, the interface input unit controlling the transmission of data cells from the external processing system to the input buffer memory unit;

an output buffer memory unit, the output buffer memory unit receiving data cells from the direct memory access unit;

an interface output unit, the interface output unit controlling transmission of data cells from the output buffer memory unit to the external processing system; and

a clock detection unit, the clock detection unit generating a least one control signal when the external clock signal is not present.

13. The interface unit of claim 12 wherein the clock detection unit includes a counter and a register, the counter having internal clock signals applied to an input terminal thereof, the counter having the external clock signal applied to a reset terminal thereof, the register coupled to the counter to determined the number of internal clock signals to be counted before the external clock signals was determined to be missing.

14. The interface unit as recited in claim 12 wherein the input and output buffer memory units are first-in/first-out memory units, the first in/first out memory uits capable of storing can store at least two data cells.

15. The interface unit as recited in claim 12 wherein the receive event signal is generated when the input buffer memory unit has a complete data cell stored therein, the receive event signal being cleared when transfer between the input buffer memory unit and the direct memory access unit is begun, and wherein the transmit event signal is generated when the output buffer memory unit has space for a complete data cell, the transmit event signal being cleared when the transfer of the data cell to the output buffer memory unit from the direct memory access unit is begun.